AN11022

CLRC663 Quickstart Guide

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Application note
COMPANY PUBLIC

Document information

Info	Content
Keywords	RC663, Reader IC, Power Supply, Interfacing RC663, RC663 Quick start up, Functional description, Register settings
Abstract	This document describes the required basic circuitry to operate the RC663 and it also describes how to set up first communication using the RC663 Design-In Board (Demo Board V 3_0)

Revision history

Rev	Date	Description
1.0	20120216	Initial release

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1. Introduction

This document describes the basic requirements to power up the reader IC. This application note does not replace the CLRC663 datasheet. Please refer to the datasheet to read more information on each chapter. This document also gives an overview of the RC663 evaluation reader board and describes the function and first steps of using the board and the RC663. For this Application Note Version 3.0 of the 663 reader board is used.

2. General description of the RC663

The RC663's overall functionality can be separated into three functions:

1. **Generate the RF field**: The generated magnetic field has to be maximized within the limits of the transmitter supply current, general emission limits and requirements to protocol standards.
2. **Transmit data**: The coded and modulated data signal has to be transmitted in a way, that all supported card standards are able to receive it. The signal shape and timing according to relevant standards has to be considered.
3. **Receive data**: The response of a card or NFC passive device has to be transferred to the differential or single sided receive input of the RC663 considering various limits, e.g. maximum voltage and receiver sensitivity.

In the following chapters the general wiring just like the power supply concept, interface selection and so on is described**.**

2.1 Basic wiring

The basic wiring diagram can be found in Fig 1. The matching procedure of the antenna can be found in the application note AN11019 (Ref. 2).

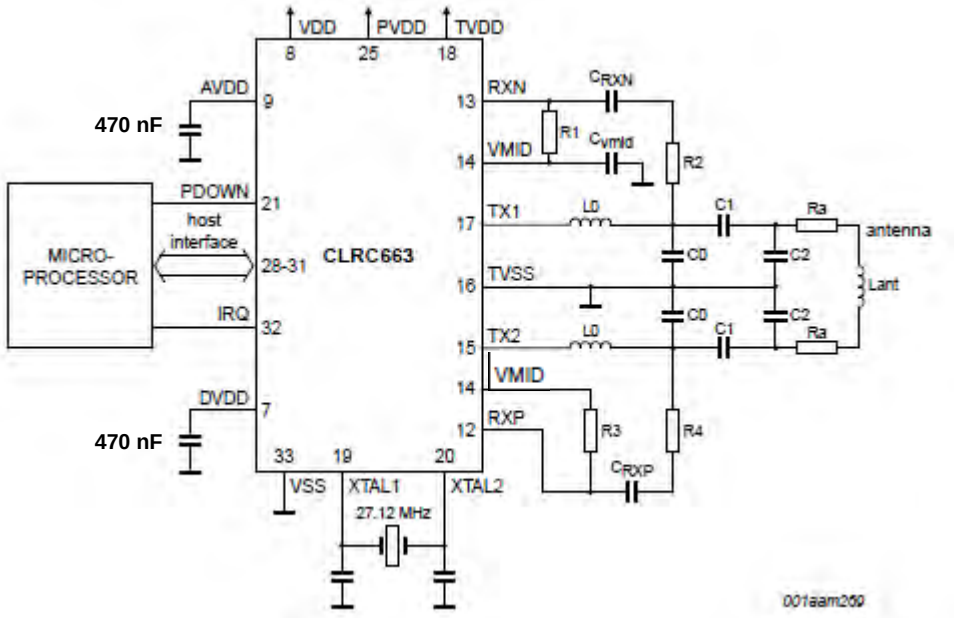


Fig 1. Basic wiring diagram

It is recommended that Input pins which are not used be tied to a defined electrical potential.

Output pins can be floating.

2.2 Power supply concept

The CLRC663 is supplied by VDD - Supply voltage, PVDD- pad supply and TVDD- Tx power supply. These three voltages are independent and can have different as well as the same supply voltage values. e.g. to operate with a 3.3 V supplied Microcontroller, PVDD and VDD shall be 3.3 V, to guarantee maximum field strength TVDD shall be 5V.

Voltages between 3 V to 5.5 V can be applied to VDD, PVDD and TVDD.

Independent of the voltage it is recommended to buffer these supplies with blocking capacitors. VDD and PVDD min 100 nF; TVDD min 100 nF parallel to 1 uF

NOTE: AVDD and DVDD are not Voltage inputs! Buffer them with blocking capacitances of 470 nF each.

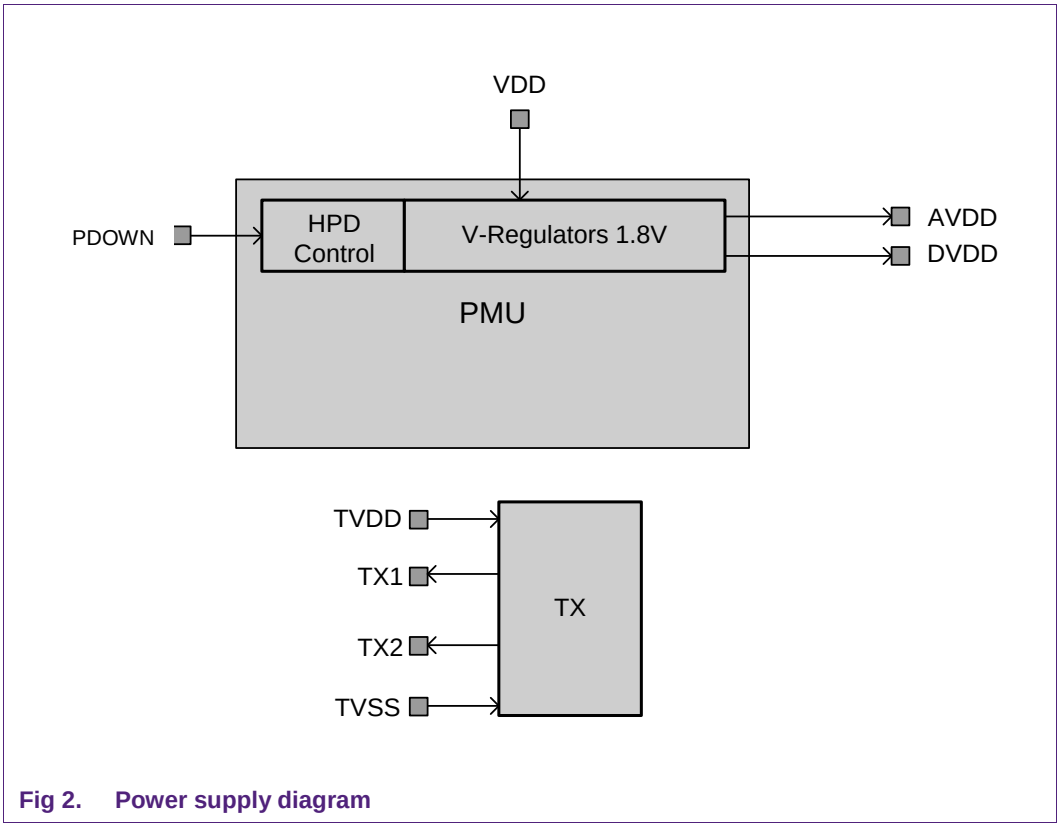


Fig 2. Power supply diagram

2.3 Interface selection

The CLRC663 supports direct interfacing of various hosts as the SPI, I2C, I2CL and serial UART interface type. The CLRC663 resets its interface and checks the current host interface type automatically having performed a Power-On or Hard Reset. The CLRC663 identifies the host interface by the means of the logic levels on the control pins after the Reset Phase. This is done by a combination of fixed pin connections IF1SEL0 and IF1SEL1. The following table shows the different configurations:

Table 1. Connection Scheme for detecting the different Interface Types

		UART	SPI	I2C	I2C-L
IF0	I/O	Rx	MOSI	ADR1	ADR1
IF1(SCL)	I/O		SCK	SCL	SCL
IF2	I/O	Tx	MISO	ADR2	SDA
IF3-SDA	SDA	Trigger	NSS	SDA	ADR2
IFSEL0	I	0	0	1	1
IFSEL1	I	0	1	0	1

2.4 Crystal oscillator

The clock applied to the CLRC663 acts as a time basis for generation of the carrier sent out at TX, for the quadrature mixer I and Q clock generation, and for the coder and decoder of the synchronous system. Therefore, stability of the clock frequency is an important factor for proper performance. To obtain highest performance, clock jitter has to be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry.

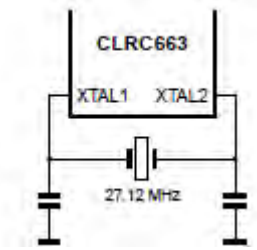


Fig 3. Crystal connection

Table 2. Crystal requirements recommendations

Symbol	Parameter	min	Typ	max	Unit
fxtal	Crystal frequency		27.12		MHz
Δfxtal	Crystal frequency accuracy	-250		+250	ppm
ESR	Equivalent series resistant		50	100	Ω
CL	Load capacitance		10		pF
Pxtal	Crystal power dissipation		50	100	uW

2.5 Receiver circuit

The **Receiver is a fully** differential circuit and can be used double ended or single ended:

- ➔ **For single ended** use (Quasi- Differential) of the receiver circuit it is strongly recommended to connect RxN and RxP to each other or to connect them by using the Rcv_Reg register (address 38h).But if the Rcv_Rx_single bit in the Rcv_Reg register is set to 1 -> Quasi-Differential, the unused Rx pin has to be open and not connected to Ground.
- ➔ **For double ended** use connect RxN and RxP, as recommended, to the transmitter circuit, directly after the EMC filter.

3. Hardware design of the RC663 evaluation board (“red board”)

3.1 Scope

This part describes the functionality of the evaluation reader based on the RC663. It includes the functional and electrical specifications and gives the needed details to use this reader as a reference design.

This reader implementation is based on the HVQFN33 package (body 5 x 5 x 0.85 mm).

The RC663 itself is described in the corresponding data sheet (see reference [1]).

3.2 Features

- Single 7.5 V external power supply
- RS232 DSUB9 connector for easy connection to a host PC
- RS232 Serial UART up to 1228.8 kBd, with voltage levels dependent on pin voltage supply
- Supports transfer speed communication up to 848 kbit/s with credentials
- I/O pins (GPIO0/SIGIN; SIGOUT)
- Hard Power Down
- Standby mode
- Programmable and cascadable timers
- FiFo buffer handles 512 byte send and receive
- IntegerN PLL providing clock for standard microcontroller used frequencies
- Low power card detection
- Integrated Free-Running Low Power Oscillator
- Digital test signal pins CLKOUT,SIGOUT,TCK,TDI,TDO,TMS
- versatile quadrature receiver architecture with fully differential receiver
- Antenna size: 113 mm x 77 mm

3.3 Functional description

The RC663 evaluation reader is a contactless smartcard reader based on the RC663 reader IC.

The Reader PCB is divided into 2 Parts, the general reader part and The Antenna and matching part:

Table 3. PCB sections

PCB Section	Description
General reader part (Fig 5 lower figure)	Includes Power supply, Rs232 Interface and RC663 related part also EMC filter for TX circuit
Antenna and matching part (Fig 5 lower figure)	Antenna matching (without EMC filter) with fully differential receiver circuit and PCB antenna coil

The reader has one drawn cutline between EMC filter and matching circuit. This is to cut the antenna and the antenna related matching from the reader (Fig 4). Seven vias have been added to connect another Antenna with matching to the evaluation reader.

Fig 4. RC663 board version 3.0

3.4 PCB Marking and major improvements to older version

There are two versions of the RC663 board version 2.0 and version 3.0

The latest version is:

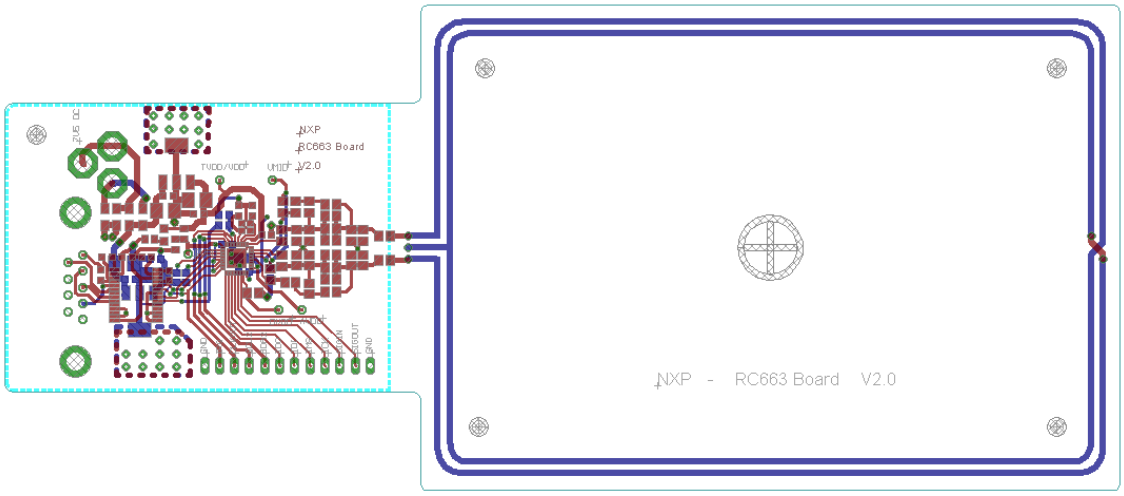
NXP

RC663 Board V3.0

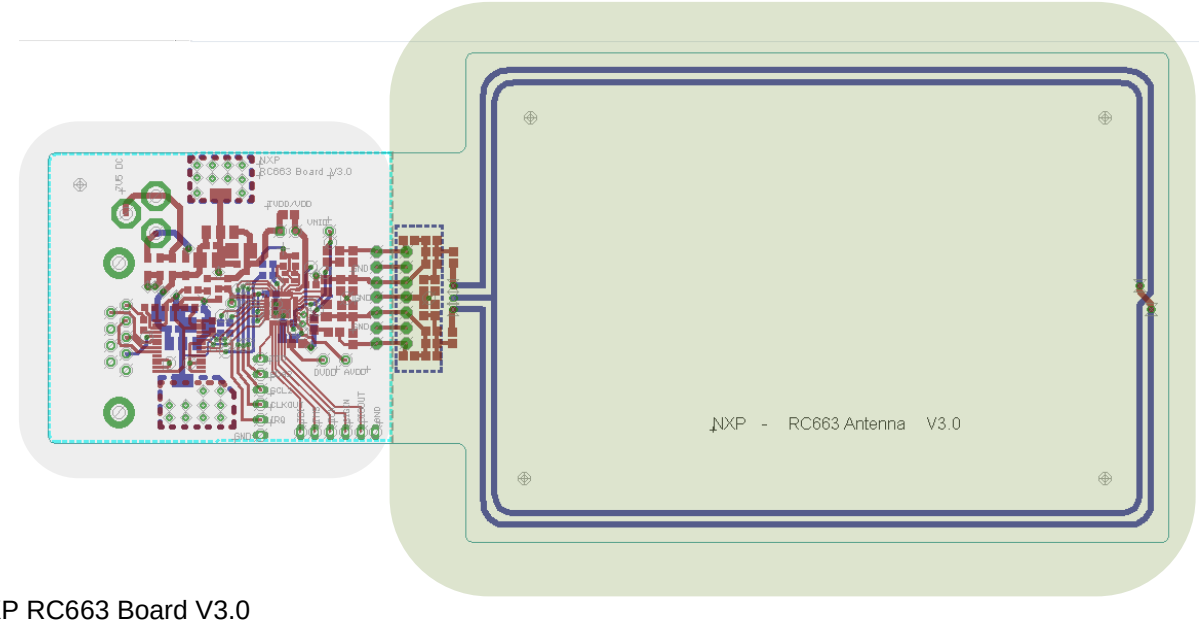
The difference is shown below (Fig 5)

Improvements form V 2.0 to V 3.0:

- ➔ Adding a Cutline to separate the general reader part from the Antenna and matching part
- ➔ Analog debug pins are outlined
- ➔ Adding pins for current measurement on TVDD
- ➔ Prepared for adding another antenna with matching



NXP RC663 Board V2.0



NXP RC663 Board V3.0

Fig 5. NXP RC663 Board V2.0 and 3.0

3.5 Schematic description

The following parts describe the RC663 evaluation reader board schematic, the part list, and the layout of the PCB completely in order to give the user the possibility to take the evaluation reader as a reference design for contactless smartcard reader integration.

3.6 Interface section

3.6.1 Power supply

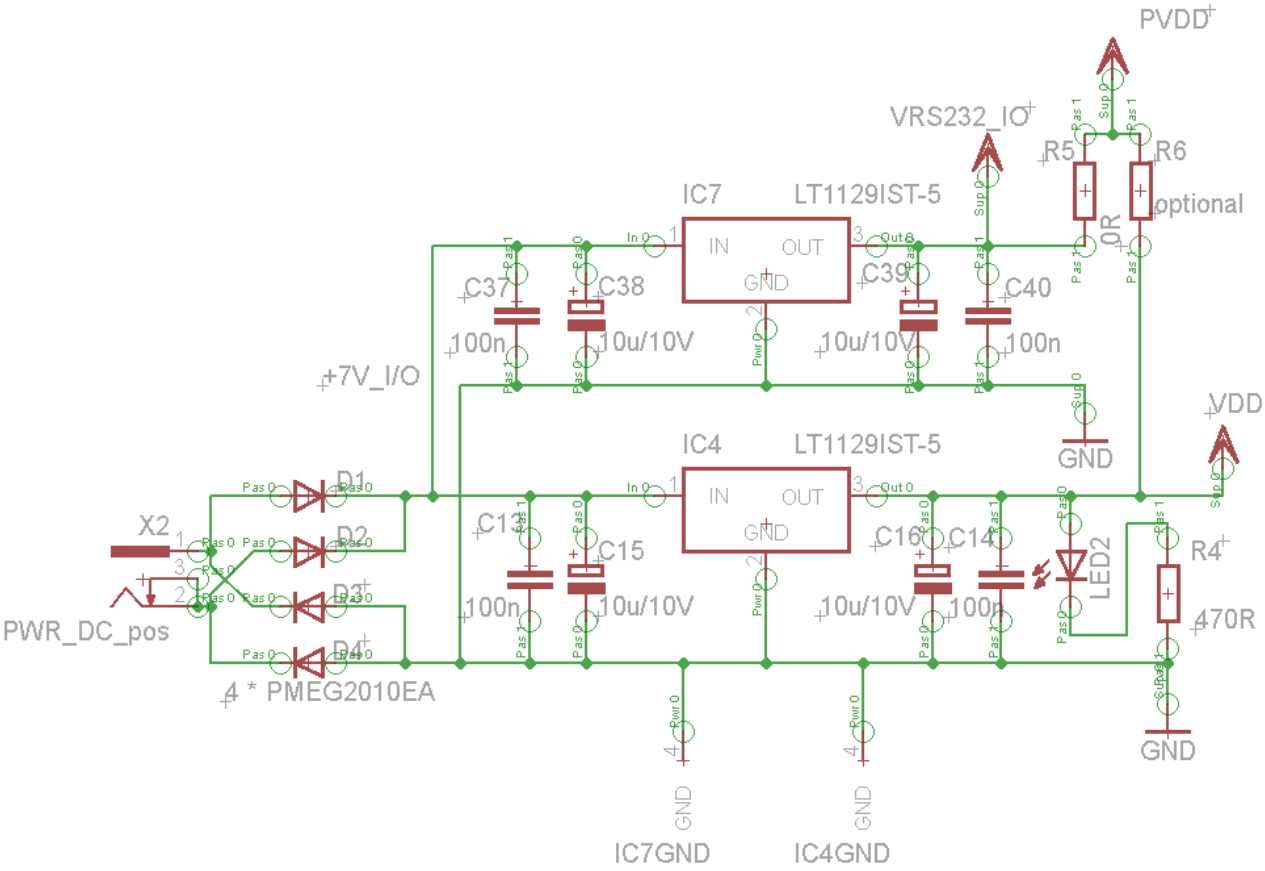


Fig 6. Power supply circuit

The power supply can be connected with a 2.5 mm dc plug. The polarity of the plug is managed automatically on the PCB. The supplied voltage should be in a range of 7.5 V to 12.0 V and can be unregulated. The power supply should be able to provide at least 250 mA.

The main supply voltage at TVDD and PVDD is 5 V.
The Core supply Voltage at AVDD and DVDD is 1.8 V.

After plugging the voltage supply, the LED on the PCB should light up.

3.6.2 RS232 Host interface

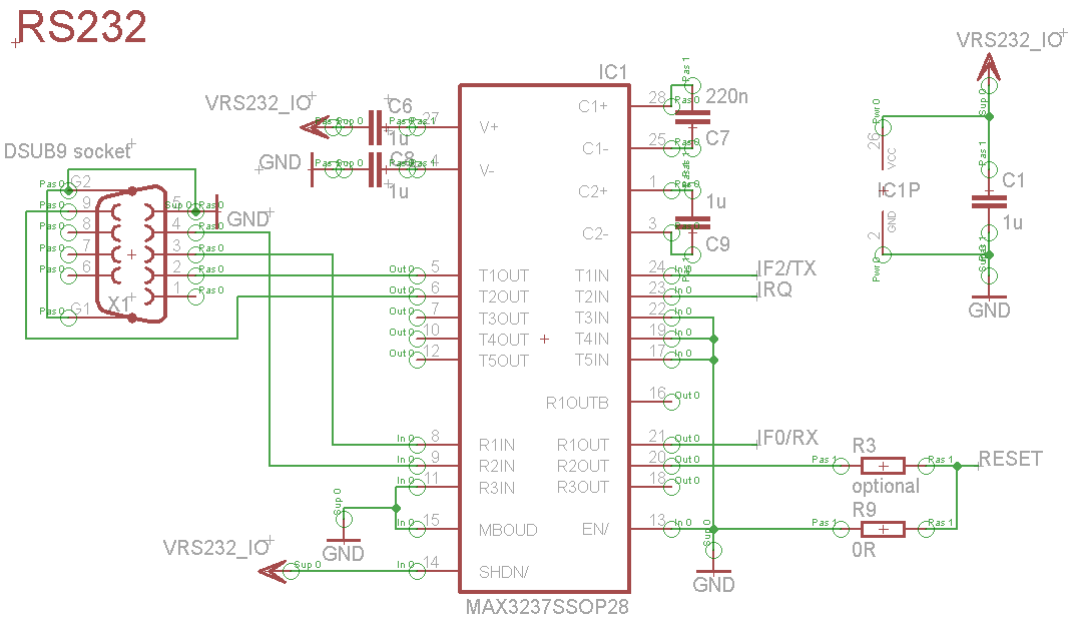


Fig 7. RS232 interface and transceiver

The DSUB-9 socket is used for a standard RS232 connection to the PC.

For this interface the following values are assembled:

Table 4. Used devices for RS232 interface

Device	Value
C1	1 µF
C6	1 µF
C7	220 nF
C8	1 µF
C9	1 µF
R3	Not assembled
R9	0 Ω

Table 5. DSUB-9 Pinning for RS232

Pin	Signal	D	Voltage
1	DCD (Data Carrier Detect)	O	± 3 – 12 V
2	RD (Receive Data)	O	± 3 – 12 V
3	TD (Transmit Data)	I	± 3 – 12 V
4	DTR (Data Terminal Ready)	I	± 3 – 12 V
5	GND	Pwr	
6	DSR (Data Set Ready)	O	± 3 – 12 V
7	RTS (Ready To Send)	I	± 3 – 12 V
8	RTS (Ready To Send)	O	± 3 – 12 V
9	RI (IRQ)	O	± 3 – 12 V

3.6.3 Microcontroller interface type

The CLRC663 supports direct interfacing of various hosts as the SPI, I2C, I2CL and serial

UART interface type. The CLRC663 resets its interface and checks the current host interface type automatically having performed a Power-On or Hard Reset. The CLRC663 identifies the host interface by the means of the logic levels on the control pins after the Reset Phase. This is done by a combination of fixed pin connections. The Table 1 on page 5 shows the different configurations.

3.6.4 USB-RS232 adapter

The development boards make use of a serial RS232 interface which is connected to a PC to execute scripts or other PC based software to control the functionality of the contactless reader IC.

More and more it is found that modern PC's are not equipped by default with the RS232 interface.
A standard interface available on most PCs is the USB interface. USB to serial converters convert the signals of a USB interface to RS232 signals are available in the market.
In practice we have found that not all USB /RS232 converters are working without problems. The reason for this problem could be that the designers of this interface need to find a compromise to fit most applications, so that it does not fit very well to the use case of transferring contactless data.

To avoid this problem more information's about RS232 to USB converter and the right configuration can be found in AN11116 ("Using the RS232 serial evaluation boards on a USB port") on CLRC 663 web page.

3.6.5 RC663 schematic

This part shows a short overview of the RC336 schematic with all connections and also the oscillator part of the evaluation reader.

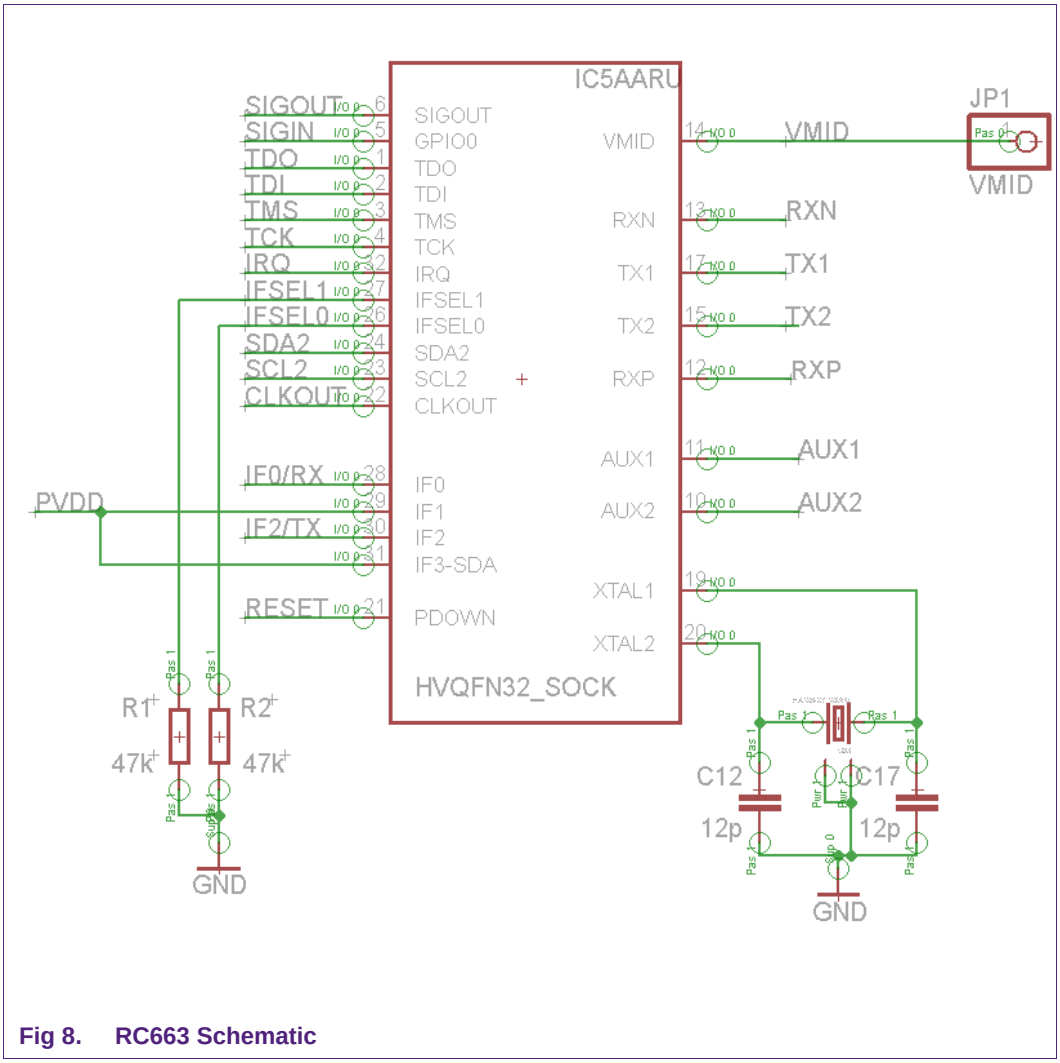


Fig 8. RC663 Schematic

Table 6. Used devices for RC663 Schematic including oscillator

Device	Value
R1 / R2	47 kΩ
Quarz	EPSON TOYOCOM - FA-128, 27.120000 MHZ, +-15PPM - QUARZ ,FA-128,27.120000 MHZ,+-15PPM
C12	12 pF

3.6.6 Antenna circuit

The Transceiver circuit is divided into 3 Parts: the Antenna, Matching Circuit, and EMC Filter. The matching part of the transceiver circuit is responsible for the matching resistance of the whole Tx circuit. To tune your Antenna to the target resistance C1 and C2 have to be adjusted. For more information's about Antenna design and Tuning see AN11019 ("CLRC Antenna Design Guide") and AN78010 ("13.56 MHz RFID Proximity Antennas").

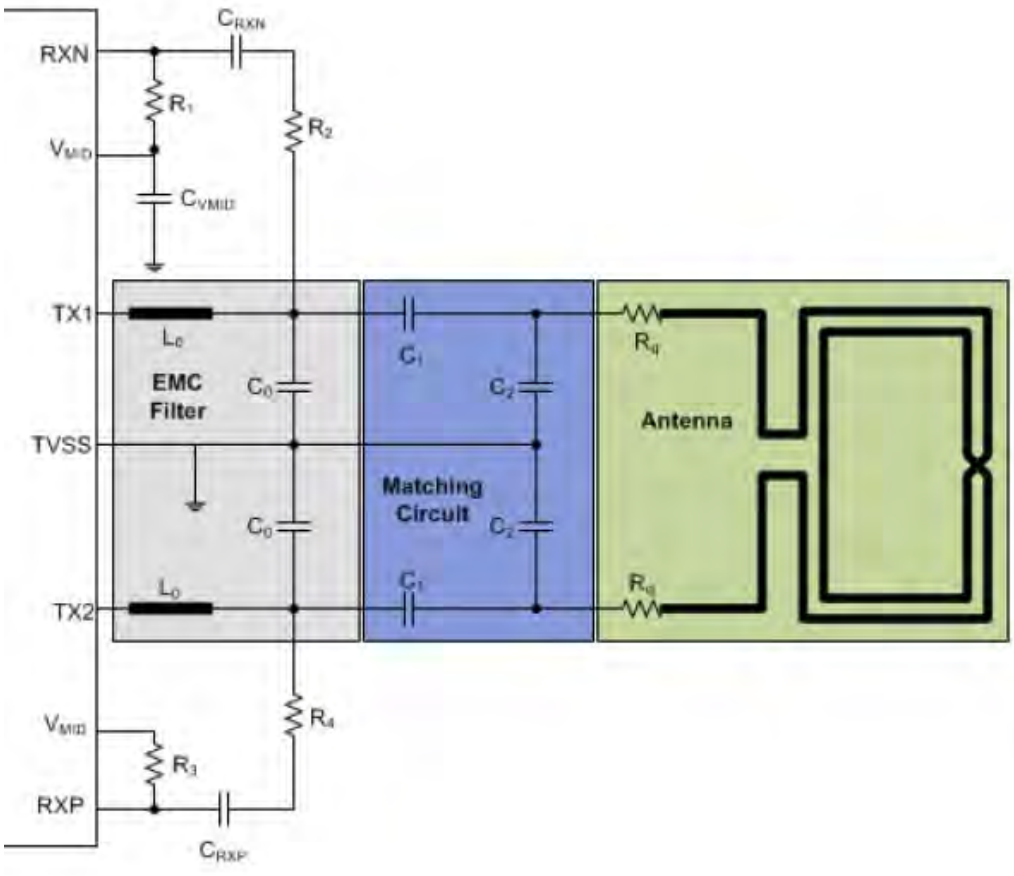


Fig 9. Antenna and transceiver circuit

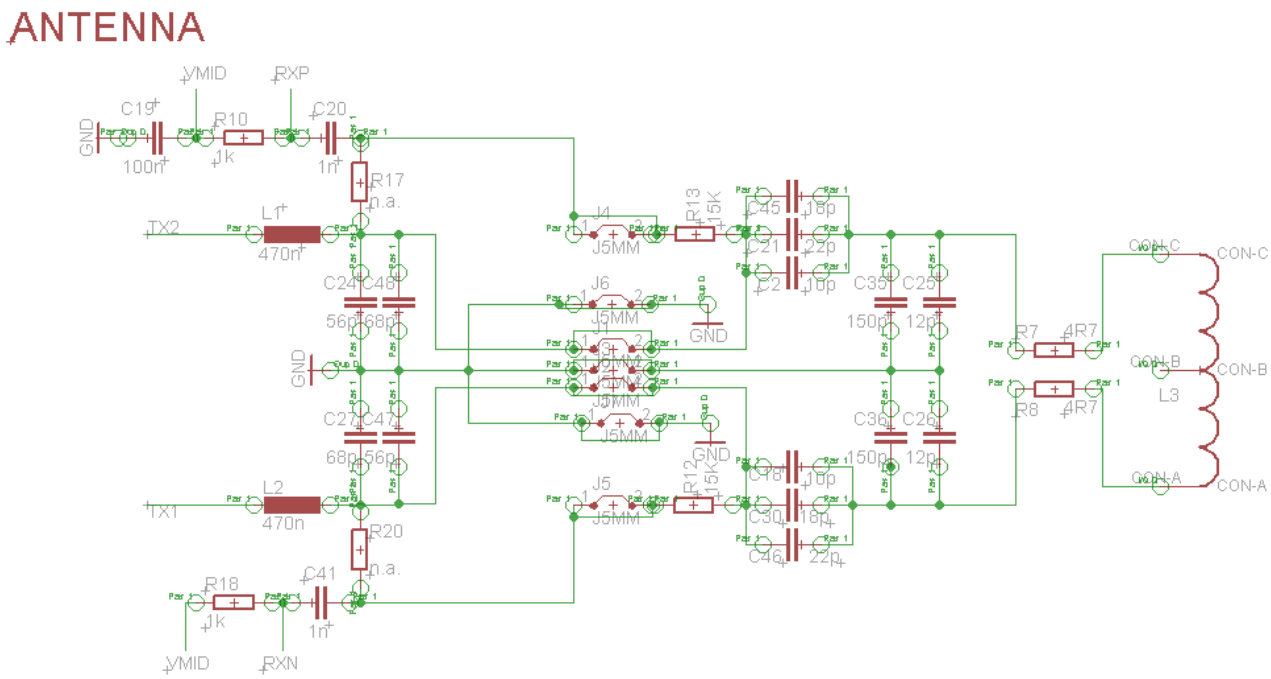


Fig 10. Schematic of the Antenna and Transceiver circuit

Table 7. Used devices for RC663 Schematic including oscillator

	Device	Value
R_q	R7 / R8 *Damping Resistors for Q limitation*	4,7 Ω
C_2	C25	12 pF
	C26	12 pF
	C35	150 pF
	C36	150 pF
C1	C2	10 pF
	C18	10 pF
	C21	22 pF
	C30	18 pF
	C45	18 pF
	C46	22 pF
EMC	L1	470 nH *WE-MK 0.47uH 200mA, manufacturer Würth Elektronik; manufacturer. part-nr. 74479032*
	L2	470 nH *WE-MK 0.47uH 200mA, manufacturer Würth Elektronik; manufacturer. part-nr. 74479032*

	Device	Value
	C24	56 pF
	C27	68 pF
	C47	56 pF
	C48	68 pF
Receiver circuit	R12	15 kΩ
	R13	15 kΩ
	R17	n.A.
	R20	n.A.
	C19	100 nF
	C20	1 nF
	C41	1 nF
	R10	1 kΩ
	R18	1 kΩ

3.7 PCB description and functionality

3.7.1 Top layer and placing

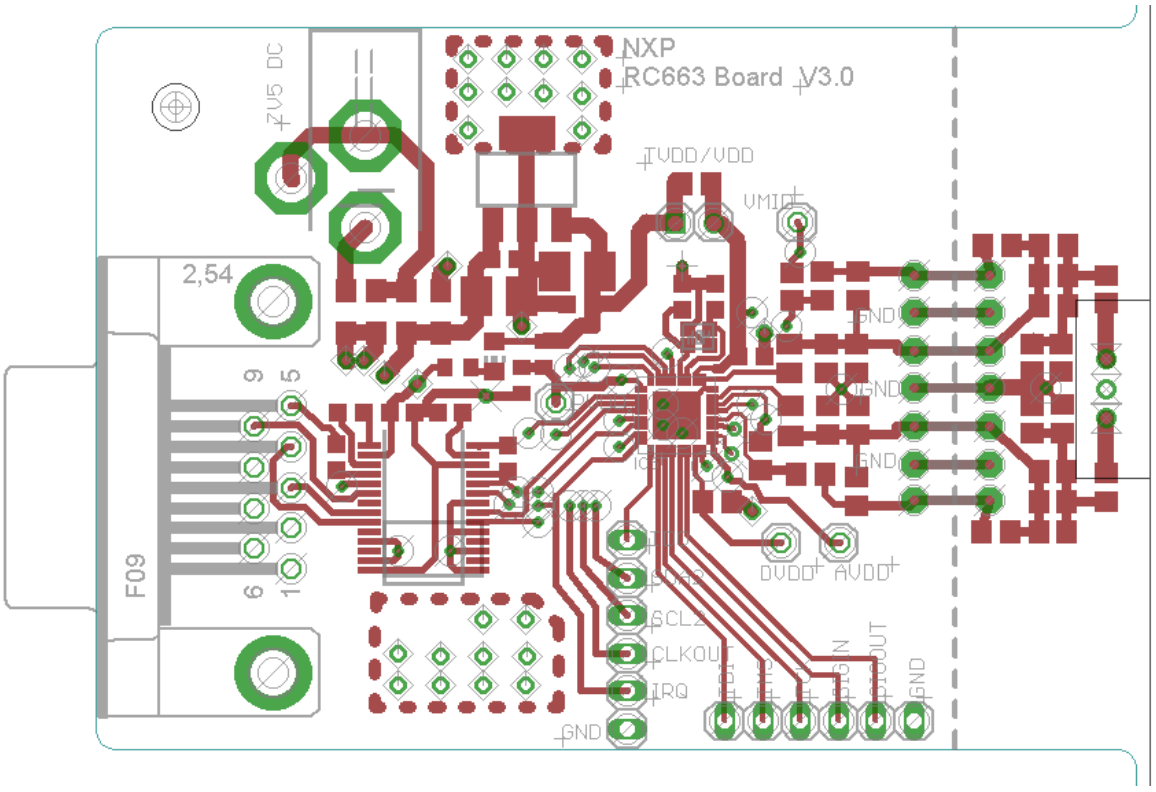


Fig 11. Top layer RC663 board

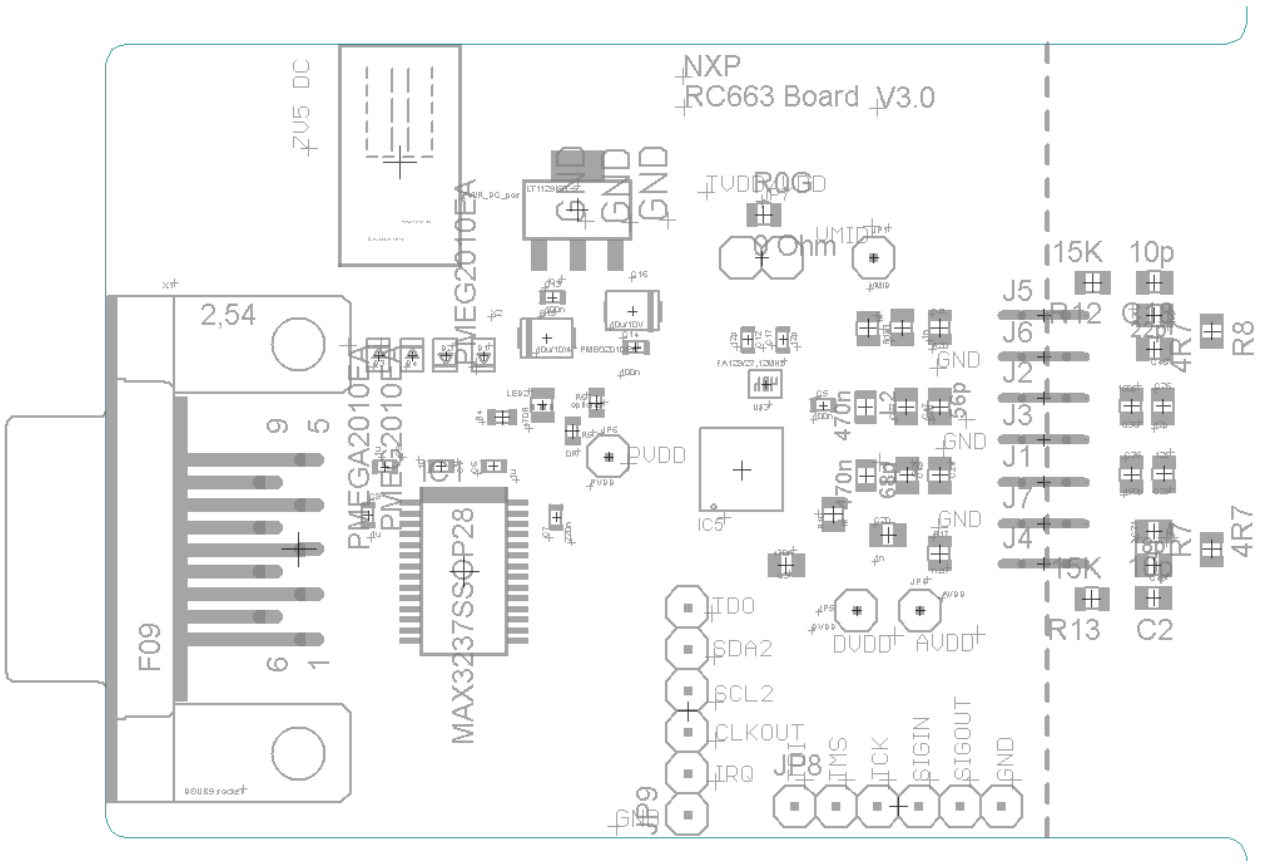


Fig 12. Parameter Selection Placement Top Layer

3.7.2 Bottom, middle layer and placing

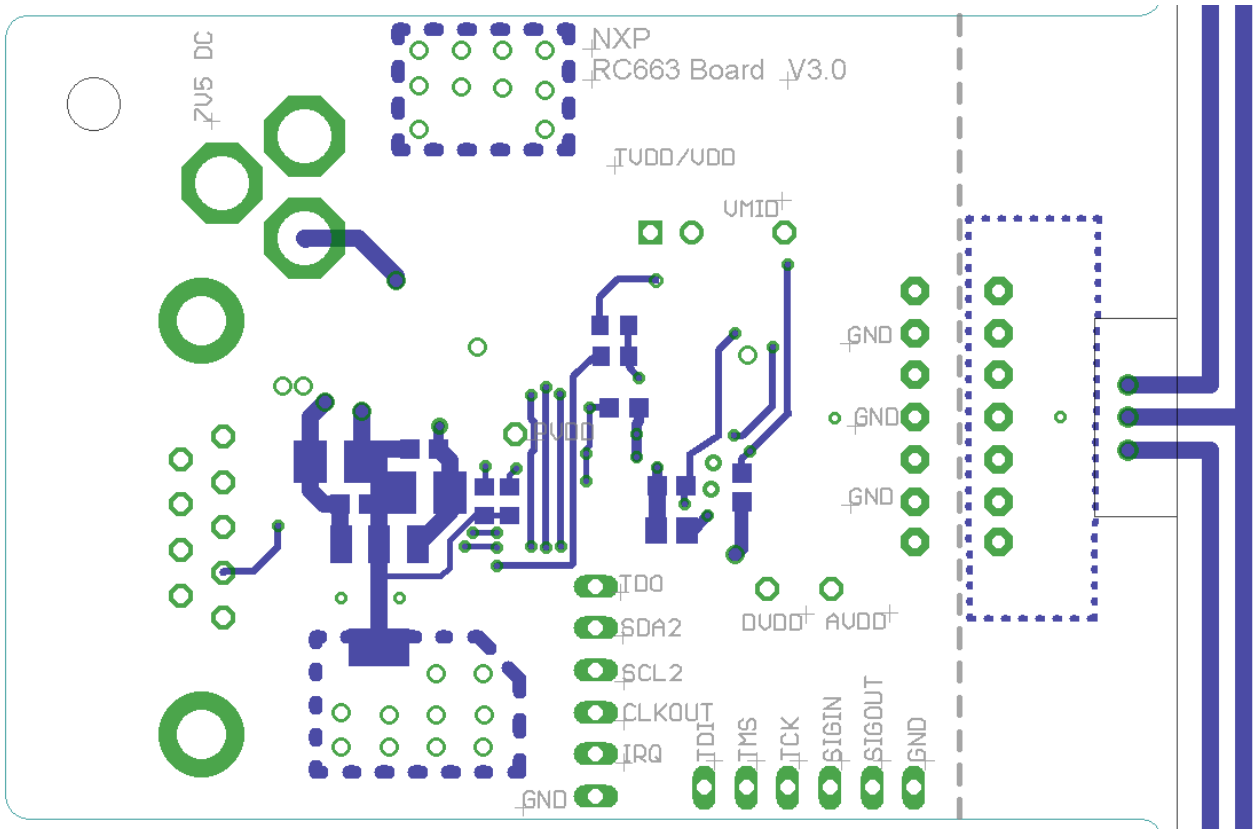


Fig 13. Bottom layer RC663 board

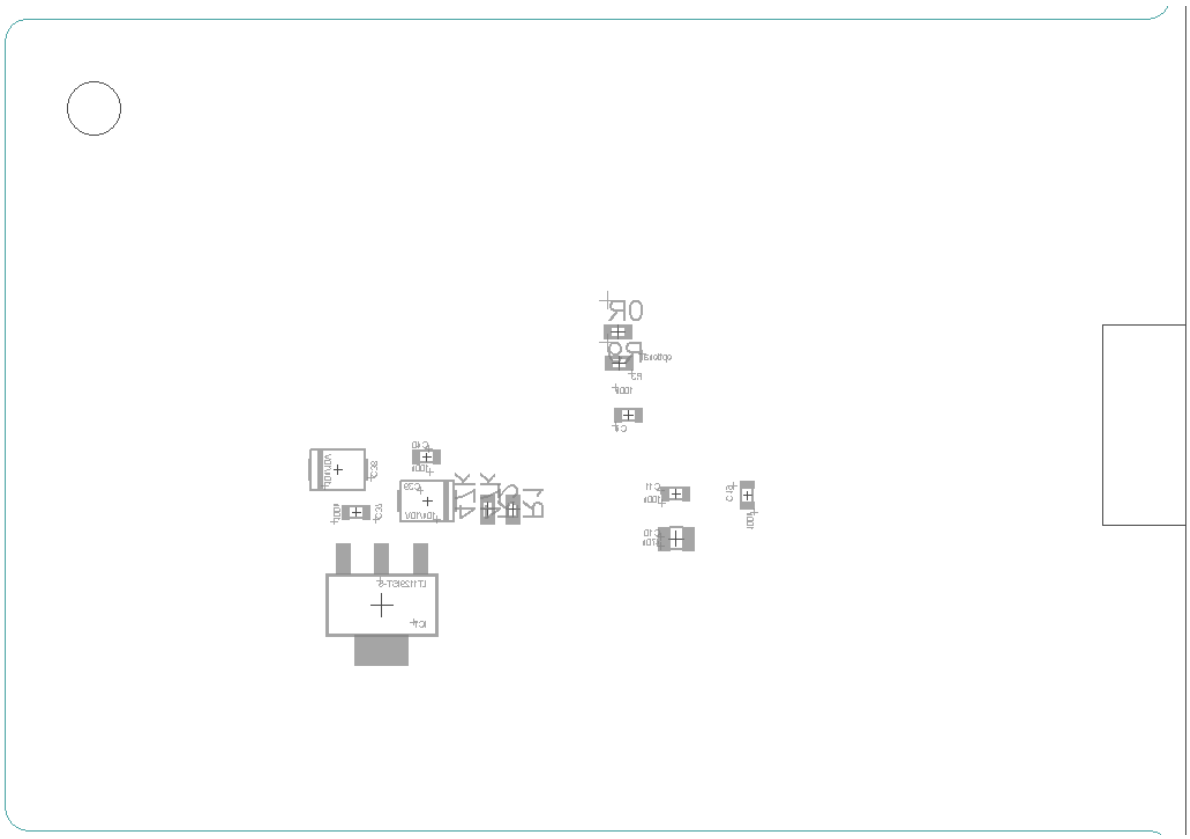


Fig 14. Placement bottom Layer

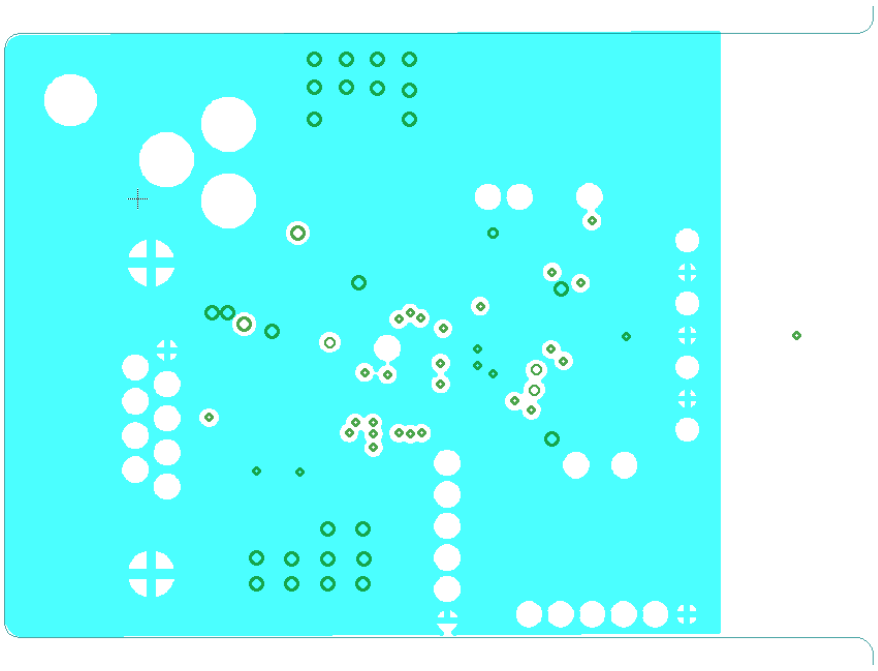


Fig 15. Middle layer RC663 board

3.7.3 PCB antenna section

Refer to section 3.6.6

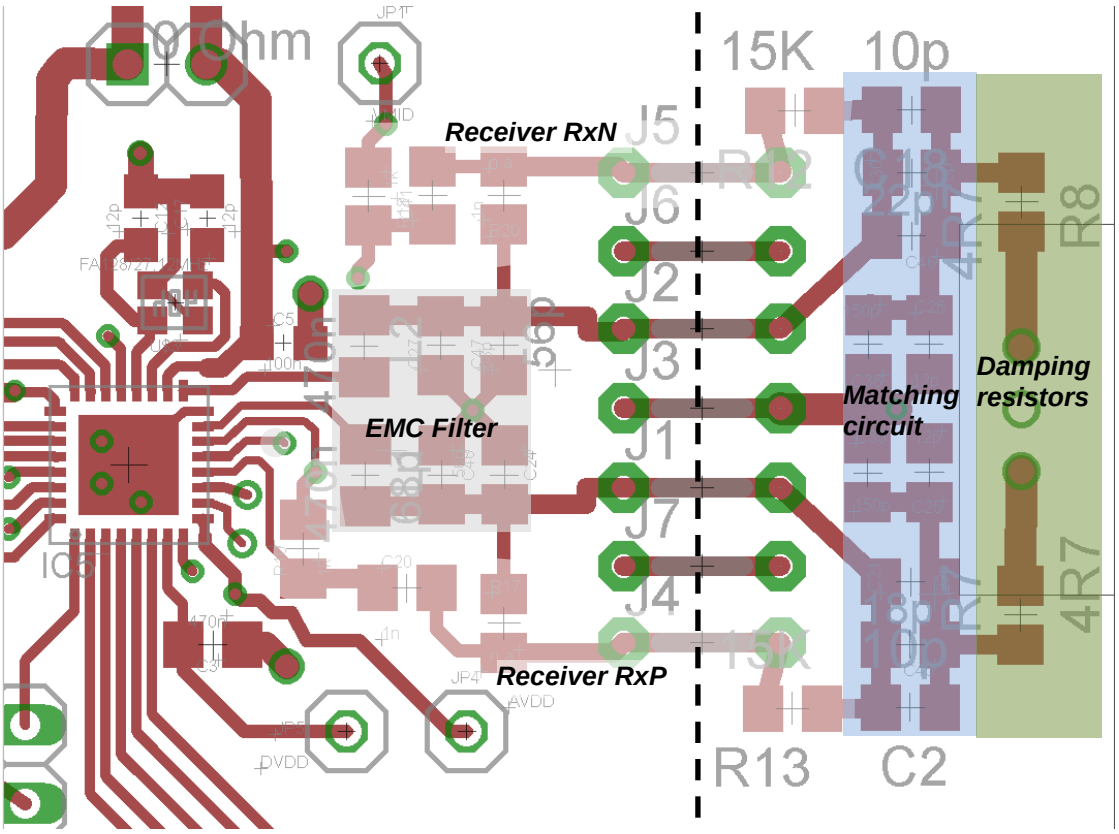


Fig 16. PCB antenna section

The matching circuit and the antenna with damping resistor part of the RC663 board can be separated by cutting the board along the white dashed line on the top side of the board. This line is shown in black in Fig 16. The EMC filter is left on the board. After cutting the antenna and matching circuit the receiver resistor, for the voltage divider, R12 and R13 (these resistors are also on the antenna and matching side) can be replaced by using R17 and R20. Both resistors are not assembled, they are only for the case that the antenna section is cut from the reader part.

To connect a different antenna, J1-J7 can be used (after cutting the board).

Table 8. Antenna section connector

Connector via	Signal
J1	Tx2
J2	Tx1
J3	GND
J4	RxP
J5	RxN
J6	GND
J7	GND

4. Register Settings for different modes and features

4.1 EMD suppression

The EMD suppression feature is only for ISO 14443 use cases.

If an error occurs within the first three bytes or the frame is < 3 bytes, this frame is seen as EMD and ignored. If RxForceCRCWrite is set, the FIFO should not be read out before three bytes are written into. The FIFO is cleared automatically in case of an EMD error. A collision is treated as error.

To activate the EMD suppression the EMD_SUP Bit in the RxCtrl Register has to be set. (Table 9)

Table 9. RxCtrl_Reg register (address 35h); reset value: 04h

Bit	7	6	5	4	3	0 - 2
Symbol	RxAllow Bits	Rx Multiple	RxEOF Type	EGT_ Check	EMD_ Sup	Baud rate
Access rights	r/w	r/w	r/w	r/w	r/w	r/w

4.2 Load Protocol command

The Load Protocol command reads data from the internal EEPROM and initializes the CLRC663 registers needed for a Protocol change.

The command reads out the EEPROM (RX and TX protected area) and copies the values from the RX- and TX protected area into the Registers.

The RX and TX protected area is a special area in the EEPROM with read access only.

The load protocol command loads only the values for the registers 0x48 and 0x4A – 0x5F. The command loads only these registers because they are only related to the type of protocol that is used and not hardware or software related. From this it follows that the rest of the registers, for the chosen protocol have to be set in addition (see chapter 4.3 and following).

The Parameter for the command is:

Protocol Number RX (1 byte, 0x00 - 0xFF) + Protocol Number TX (1 byte, 0x00 - 0xFF)

The following table (Table 10) is an overview over the predefined protocols that can be loaded.

Note: The predefined Values for the RX and TX Protected area are shown in the ID2 antenna charts in Chapters 4.3 and following (marked in blue).

Table 10. Predefined protocol overview

Protocol Number	Protocol	Transmitter speed [kbits/s]	Modulation	Receiver speed [kbits/s]	Modulation
00	ISO/IEC14443 A	106	Miller	106	Manchester SubC
01	ISO/IEC14443 A	212	Miller	212	BPSK
02	ISO/IEC14443 A	424	Miller	424	BPSK
03	ISO/IEC14443 A	848	Miller	848	BPSK
04	ISO/IEC14443 B	106	NRZ	106	BPSK
05	ISO/IEC14443 B	212	NRZ	212	BPSK
06	ISO/IEC14443 B	424	NRZ	424	BPSK
07	ISO/IEC14443 B	848	NRZ	848	BPSK
08	FeliCa	212	Manchester	212	Manchester
09	FeliCa	424	Manchester	424	Manchester
10	ISO/IEC15693		¼		SSC
11	ISO/IEC15693		¼		DSC
12	ISO/IEC15693		1/256		SSC
13	EPC/UID		Unitray		SSC
14	ISO/IEC18000-3 Mode 3		Tari, ASK,PIE		2/424

Example for using the load protocol with the CLRC663 PcSerial.3.6.exe.:

```
CLL
CHB 115200

 Terminate any running command. Flush_FiFo
  SR 00 00
  SR 02 b0

// Clear all IRQ 0,1 flags
  SR 06 7f
  SR 07 7f

//> Write in Fifo: Tx and Rx protocol numbers(0,0)
  GR 04
  SR 05 04   // Rx protocol=0
  SR 05 04    // Tx prot=0

// Enable IRQ0 interrupt sources
//
// Idle interrupt(Command terminated), RC663_BIT_IDLEIRQ=0x10
  GR 08
  SR 08 10

// Enable Global IRQ propagation.
  GR 09
  SR 09 40

//> Start RC663 command "Load Protocol"=0x0d
  SR 00 0D

  ::: L_LoadProtocol
  GR  07
  JNM IOR 40 40 L_LoadProtocol

// Disable Irq 0,1 sources
  SR 08 00
```

SR 09 00

//> Flush Fifo. Read Error Reg

SR 02 B0

GR 0A

4.3 ISO/IEC 14443 Type A recommended register settings

The following section gives an overview of the recommended register settings for ISO/IEC 14443 Type A communication, with different Antenna sizes (ID1, ID2, ID3).

4.3.1 ISO/IEC 14443 Type A for ID1 sized antenna

Table 11. Register settings Type A ID1 sized antenna

Reg	Reg descr	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
28	DrvMode_Reg	0x8A	0x8E	0x8E	0x8F
29	TxAmp_Reg	0x08	0x5C	0x5C	0x9E
2A	DrvCon_Reg	0x21	0x01	0x01	0x01
2B	TxI_Reg	0x1A	0x0A	0x0A	0x0A
2C	TXCrcCon	0x18	0x18	0x18	0x18
2D	RxCrcCon	0x18	0x18	0x18	0x18
2E	TxDataNum	0x0F	0x0F	0x0F	0x0F
2F	TxModWidth	0x27	0x10	0x08	0x03
30	TxSym10BurstLen	0x00	0x00	0x00	0x00
31	TxWaitCtrl	0xC0	0xC0	0xC0	0xC0
32	TxWaitLo	0x12	0x12	0x12	0x12
33	TxFrameCon	0xCF	0xCF	0xCF	0xCF
34	RXSOFD	0x00	0x00	0x00	0x00
35	RxCtrl	0x04	0x05	0x06	0x07
36	RxWait	0x90	0x90	0x90	0x90
37	RxTreshold	0x32	0x32	0x32	0x32
38	Rcv	0x12	0x12	0x12	0x12
39	RxAna	0x0A	0x02	0x02	0x02
48	TxBitMod	0x20	0x20	0x20	0x20
4A	TxDataCon	0x04	0x05	0x06	0x07
4B	TxDataMod	0x50	0x50	0x50	0x50
4C	TxSymFreq	0x40	0x50	0x60	0x70
4D	TxSym0H	0x00	0x00	0x00	0x00
4E	TxSym0L	0x00	0x00	0x00	0x00
4F	TxSym1H	0x00	0x00	0x00	0x00
50	TxSym1L	0x00	0x00	0x00	0x00
51	TxSym2	0x00	0x00	0x00	0x00
52	TxSym3	0x00	0x00	0x00	0x00
53	TxSym10Len	0x00	0x00	0x00	0x00
54	TxSym32Len	0x00	0x00	0x00	0x00
55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
56	TxSym10Mod	0x00	0x00	0x00	0x00
57	TxSym32Mod	0x50	0x50	0x50	0x50
58	RxBitMod	0x02	0x22	0x22	0x22
59	RxEofSym	0x00	0x00	0x00	0x00
5A	RxSyncValH	0x00	0x00	0x00	0x00
5B	RxSyncValL	0x01	0x00	0x00	0x00
5C	RxSyncMod	0x00	0x00	0x00	0x00
5D	RxMod	0x08	0x0D	0x0D	0x0D
5E	RxCorr	0x80	0x80	0x80	0x80
5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

4.3.2 ISO/IEC 14443 Type A for ID2 sized antenna

Table 12. Register settings Type A ID2 sized antenna

	Reg	Reg descr	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
	28	DrvMode_Reg	0x8A	0x8E	0x8E	0x8F
	29	TxAmp_Reg	0x08	0x12	0x12	0xDB
	2A	DrvCon_Reg	0x21	0x11	0x11	0x11
	2B	TxI_Reg	0x1A	0x06	0x06	0x06
	2C	TXCrcCon	0x18	0x18	0x18	0x18
	2D	RxCrcCon	0x18	0x18	0x18	0x18
	2E	TxDataNum	0x0F	0x0F	0x0F	0x0F
	2F	TxModWidth	0x27	0x10	0x08	0x02
	30	TxSym10BurstLen	0x00	0x00	0x00	0x00
	31	TxWaitCtrl	0xC0	0xC0	0xC0	0xC0
	32	TxWaitLo	0x12	0x12	0x12	0x12
	33	TxFrameCon	0xCF	0xCF	0xCF	0xCF
	34	RXSOFD	0x00	0x00	0x00	0x00
	35	RxCtrl	0x04	0x05	0x06	0x07
	36	RxWait	0x90	0x90	0x90	0x90
	37	RxTreshold	0x32	0x3F	0x3F	0x3F
	38	Rcv	0x12	0x12	0x12	0x12
	39	RxAna	0x0A	0x02	0x0A	0x02
TX_Protected	48	TxBitMod	0x20	0x20	0x20	0x20
TX_Protected	4A	TxDataCon	0x04	0x05	0x06	0x07
TX_Protected	4B	TxDataMod	0x50	0x50	0x50	0x50
TX_Protected	4C	TxSymFreq	0x40	0x50	0x60	0x70
TX_Protected	4D	TxSym0H	0x00	0x00	0x00	0x00
TX_Protected	4E	TxSym0L	0x00	0x00	0x00	0x00
TX_Protected	4F	TxSym1H	0x00	0x00	0x00	0x00
TX_Protected	50	TxSym1L	0x00	0x00	0x00	0x00
TX_Protected	51	TxSym2	0x00	0x00	0x00	0x00
TX_Protected	52	TxSym3	0x00	0x00	0x00	0x00
TX_Protected	53	TxSym10Len	0x00	0x00	0x00	0x00
TX_Protected	54	TxSym32Len	0x00	0x00	0x00	0x00
TX_Protected	55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
TX_Protected	56	TxSym10Mod	0x00	0x00	0x00	0x00
TX_Protected	57	TxSym32Mod	0x50	0x50	0x50	0x50
RX_Protected	58	RxBitMod	0x02	0x22	0x22	0x22
RX_Protected	59	RxEofSym	0x00	0x00	0x00	0x00
RX_Protected	5A	RxSyncValH	0x00	0x00	0x00	0x00
RX_Protected	5B	RxSyncValL	0x01	0x00	0x00	0x00
RX_Protected	5C	RxSyncMod	0x00	0x00	0x00	0x00
RX_Protected	5D	RxMod	0x08	0x0D	0x0D	0x0D
RX_Protected	5E	RxCorr	0x80	0x80	0x80	0x80
RX_Protected	5F	RxSvette_Reg	0xF0	0xB2	0xB2	0xB2

4.3.3 ISO/IEC 14443 Type A for ID3 sized antenna

Table 13. Register settings Type A ID3 sized antenna

Reg	Reg descr	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
28	DrvMode_Reg	0x8E	0x8E	0x8E	0x8F
29	TxAmp_Reg	0x0F	0x0F	0x0F	0xDD
2A	DrvCon_Reg	0x21	0x21	0x21	0x11
2B	TxI_Reg	0x0A	0x0A	0x0A	0x0a
2C	TXCrcCon	0x18	0x18	0x18	0x18
2D	RxCrcCon	0x18	0x18	0x18	0x18
2E	TxDataNum	0x0F	0x0F	0x0F	0x0F
2F	TxModWidth	0x27	0x10	0x08	0x02
30	TxSym10BurstLen	0x00	0x00	0x00	0x00
31	TxWaitCtrl	0xC0	0xC0	0xC0	0xC0
32	TxWaitLo	0x12	0x12	0x12	0x12
33	TxFrameCon	0xCF	0xCF	0xCF	0xCF
34	RXSOFD	0x00	0x00	0x00	0x00
35	RxCtrl	0x04	0x05	0x06	0x07
36	RxWait	0x90	0x90	0x90	0x90
37	RxTreshold	0x32	0x32	0x32	0x32
38	Rcv	0x12	0x12	0x12	0x12
39	RxAna	0x0A	0x02	0x02	0x02
48	TxBitMod	0x20	0x20	0x20	0x20
4A	TxDataCon	0x04	0x05	0x06	0x07
4B	TxDataMod	0x50	0x50	0x50	0x50
4C	TxSymFreq	0x40	0x50	0x60	0x70
4D	TxSym0H	0x00	0x00	0x00	0x00
4E	TxSym0L	0x00	0x00	0x00	0x00
4F	TxSym1H	0x00	0x00	0x00	0x00
50	TxSym1L	0x00	0x00	0x00	0x00
51	TxSym2	0x00	0x00	0x00	0x00
52	TxSym3	0x00	0x00	0x00	0x00
53	TxSym10Len	0x00	0x00	0x00	0x00
54	TxSym32Len	0x00	0x00	0x00	0x00
55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
56	TxSym10Mod	0x00	0x00	0x00	0x00
57	TxSym32Mod	0x50	0x50	0x50	0x50
58	RxBitMod	0x02	0x22	0x22	0x22
59	RxEofSym	0x00	0x00	0x00	0x00
5A	RxSyncValH	0x00	0x00	0x00	0x00
5B	RxSyncValL	0x01	0x00	0x00	0x00
5C	RxSyncMod	0x00	0x00	0x00	0x00
5D	RxMod	0x08	0x0D	0x0D	0x0D
5E	RxCorr	0x80	0x80	0x80	0x80
5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

4.4 ISO/IEC 14443 Type B recommended register settings

The following section gives an overview of the recommended register settings for ISO/IEC 14443 Type B communication, with different Antenna sizes (ID1, ID2, ID3).

4.4.1 Type B for ID1 sized antenna

Table 14. Register settings Type B ID1 sized antenna

Reg	Reg descr	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
28	DrvMode_Reg	0x8F	0x8F	0x8F	0x8F
29	TxAmp_Reg	0x4F	0x4F	0x4F	0x4F
2A	DrvCon_Reg	0x01	0x01	0x01	0x01
2B	TxI_Reg	0x0A	0x0A	0x0A	0x0A
2C	TXCrcCon	0x7B	0x7B	0x7B	0x7B
2D	RxCrcCon	0x7B	0x7B	0x7B	0x7B
2E	TxDataNum	0x08	0x08	0x08	0x08
2F	TxModWidth	0x00	0x00	0x00	0x00
30	TxSym10BurstLen	0x00	0x00	0x00	0x00
31	TxWaitCtrl	0x01	0x01	0x01	0x01
32	TxWaitLo	0x00	0x00	0x00	0x00
33	TxFrameCon	0x05	0x05	0x05	0x05
34	RXSOFD	0x00	0x00	0x00	0x00
35	RxCtrl	0x34	0x35	0x36	0x37
36	RxWait	0x90	0x90	0x90	0x90
37	RxTreshold	0x66	0x66	0x66	0x66
38	Rcv	0x12	0x12	0x12	0x12
39	RxAna	0x0A	0x02	0x02	0x02
48	TxBitMod	0x09	0x09	0x09	0x09
4A	TxDataCon	0x04	0x05	0x06	0x07
4B	TxDataMod	0x08	0x08	0x08	0x08
4C	TxSymFreq	0x04	0x05	0x06	0x07
4D	TxSym0H	0x00	0x00	0x00	0x00
4E	TxSym0L	0x03	0x03	0x03	0x03
4F	TxSym1H	0x00	0x00	0x00	0x00
50	TxSym1L	0x01	0x01	0x01	0x01
51	TxSym2	0x00	0x00	0x00	0x00
52	TxSym3	0x00	0x00	0x00	0x00
53	TxSym10Len	0xAB	0xAB	0xAB	0xAB
54	TxSym32Len	0x00	0x00	0x00	0x00
55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
56	TxSym10Mod	0x08	0x08	0x08	0x08
57	TxSym32Mod	0x00	0x00	0x00	0x00
58	RxBitMod	0x04	0x04	0x04	0x04
59	RxEofSym	0x00	0x00	0x00	0x00
5A	RxSyncValH	0x00	0x00	0x00	0x00
5B	RxSyncValL	0x00	0x00	0x00	0x00
5C	RxSyncMod	0x02	0x02	0x02	0x02
5D	RxMod	0x0D	0x0D	0x0D	0x0D
5E	RxCorr	0x80	0x80	0x80	0x80
5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

4.4.2 Type B for ID2 sized antenna

Table 15. Register settings Type B ID2 sized antenna

	Reg	Reg descr	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
	28	DrvMode_Reg	0x8F	0x8F	0x8F	0x8F
	29	TxAmp_Reg	0xCC	0xCC	0xCC	0xCC
	2A	DrvCon_Reg	0x01	0x01	0x01	0x01
	2B	TxI_Reg	0x06	0x06	0x06	0x06
	2C	TXCrcCon	0x7B	0x7B	0x7B	0x7B
	2D	RxCrcCon	0x7B	0x7B	0x7B	0x7B
	2E	TxDataNum	0x08	0x08	0x08	0x08
	2F	TxModWidth	0x00	0x00	0x00	0x00
	30	TxSym10BurstLen	0x00	0x00	0x00	0x00
	31	TxWaitCtrl	0x01	0x01	0x01	0x01
	32	TxWaitLo	0x00	0x00	0x00	0x00
	33	TxFrameCon	0x05	0x05	0x05	0x05
	34	RXSOFD	0x00	0x00	0x00	0x00
	35	RxCtrl	0x34	0x35	0x36	0x37
	36	RxWait	0x90	0x90	0x90	0x90
	37	RxTreshold	0x3F	0x3F	0x3F	0x3F
	38	Rcv	0x12	0x12	0x12	0x12
	39	RxAna	0x0a	0x02	0x09	0x02
TX_Protected	48	TxBitMod	0x09	0x09	0x09	0x09
	4A	TxDataCon	0x04	0x05	0x06	0x07
	4B	TxDataMod	0x08	0x08	0x08	0x08
	4C	TxSymFreq	0x04	0x05	0x06	0x07
	4D	TxSym0H	0x00	0x00	0x00	0x00
	4E	TxSym0L	0x03	0x03	0x03	0x03
	4F	TxSym1H	0x00	0x00	0x00	0x00
	50	TxSym1L	0x01	0x01	0x01	0x01
	51	TxSym2	0x00	0x00	0x00	0x00
	52	TxSym3	0x00	0x00	0x00	0x00
	53	TxSym10Len	0xAB	0xAB	0xAB	0xAB
	54	TxSym32Len	0x00	0x00	0x00	0x00
	55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
	56	TxSym10Mod	0x08	0x08	0x08	0x08
	57	TxSym32Mod	0x00	0x00	0x00	0x00
RX_Protected	58	RxBitMod	0x04	0x04	0x04	0x04
	59	RxEofSym	0x00	0x00	0x00	0x00
	5A	RxSyncValH	0x00	0x00	0x00	0x00
	5B	RxSyncValL	0x00	0x00	0x00	0x00
	5C	RxSyncMod	0x02	0x02	0x02	0x02
	5D	RxMod	0x0D	0x0D	0x0D	0x0D
	5E	RxCorr	0x80	0x80	0x80	0x80
	5F	RxSvette_Reg	0xB2	0xB2	0xB2	0xB2

4.4.3 Type B for ID3 sized antenna

Table 16. Register settings Type B ID3 sized antenna

Reg	Reg descr	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
28	DrvMode_Reg	0x8F	0x8F	0x8F	0x8F
29	TxAmp_Reg	0x0C	0x0C	0x0C	0x0C
2A	DrvCon_Reg	0x01	0x01	0x01	0x01
2B	TxI_Reg	0x0A	0x0A	0x0A	0x0A
2C	TXCrcCon	0x7B	0x7B	0x7B	0x7B
2D	RxCrcCon	0x7B	0x7B	0x7B	0x7B
2E	TxDataNum	0x08	0x08	0x08	0x08
2F	TxModWidth	0x00	0x00	0x00	0x00
30	TxSym10BurstLen	0x00	0x00	0x00	0x00
31	TxWaitCtrl	0x01	0x01	0x01	0x01
32	TxWaitLo	0x00	0x00	0x00	0x00
33	TxFrameCon	0x05	0x05	0x05	0x05
34	RXSOFD	0x00	0x00	0x00	0x00
35	RxCtrl	0x34	0x35	0x36	0x37
36	RxWait	0x90	0x90	0x90	0x90
37	RxTreshold	0x66	0x66	0x66	0x66
38	Rcv	0x12	0x12	0x12	0x12
39	RxAna	0x0A	0x02	0x02	0x02
48	TxBitMod	0x09	0x09	0x09	0x09
4A	TxDataCon	0x04	0x05	0x06	0x07
4B	TxDataMod	0x08	0x08	0x08	0x08
4C	TxSymFreq	0x04	0x05	0x06	0x07
4D	TxSym0H	0x00	0x00	0x00	0x00
4E	TxSym0L	0x03	0x03	0x03	0x03
4F	TxSym1H	0x00	0x00	0x00	0x00
50	TxSym1L	0x01	0x01	0x01	0x01
51	TxSym2	0x00	0x00	0x00	0x00
52	TxSym3	0x00	0x00	0x00	0x00
53	TxSym10Len	0xAB	0xAB	0xAB	0xAB
54	TxSym32Len	0x00	0x00	0x00	0x00
55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
56	TxSym10Mod	0x08	0x08	0x08	0x08
57	TxSym32Mod	0x00	0x00	0x00	0x00
58	RxBitMod	0x04	0x04	0x04	0x04
59	RxEofSym	0x00	0x00	0x00	0x00
5A	RxSyncValH	0x00	0x00	0x00	0x00
5B	RxSyncValL	0x00	0x00	0x00	0x00
5C	RxSyncMod	0x02	0x02	0x02	0x02
5D	RxMod	0x0D	0x0D	0x0D	0x0D
5E	RxCorr	0x80	0x80	0x80	0x80
5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

4.5 FeliCa recommended register settings

The following section gives an overview of the recommended register settings for FeliCa communication, with different antenna sizes (ID1, ID2, ID3).

4.5.1 FeliCa for ID1 sized antenna

Table 17. Register settings FeliCa ID1 sized antenna

Reg	Reg descr	212 kbit/s	424 kbit/s
28	DrvMode_Reg	0x8F	0x8F
29	TxAmp_Reg	0x4F	0x4F
2A	DrvCon_Reg	0x01	0x01
2B	TxI_Reg	0x0A	0x0A
2C	TXCrcCon	0x09	0x09
2D	RxCrcCon	0x09	0x09
2E	TxDataNum	0x08	0x08
2F	TxModWidth	0x00	0x00
30	TxSym10BurstLen	0x03	0x03
31	TxWaitCtrl	0x80	0x80
32	TxWaitLo	0x12	0x12
33	TxFrameCon	0x01	0x01
34	RXSOFD	0x00	0x00
35	RxCtrl	0x05	0x06
36	RxWait	0x10	0x40
37	RxTreshold	0x3C	0x3C
38	Rcv	0x12	0x12
39	RxAna	0x02	0x02
48	TxBitMod	0x80	0x80
4A	TxDataCon	0x05	0x06
4B	TxDataMod	0x01	0x01
4C	TxSymFreq	0x05	0x06
4D	TxSym0H	0xB2	0xB2
4E	TxSym0L	0x4D	0x4D
4F	TxSym1H	0x00	0x00
50	TxSym1L	0x00	0x00
51	TxSym2	0x00	0x00
52	TxSym3	0x00	0x00
53	TxSym10Len	0x0F	0x0F
54	TxSym32Len	0x00	0x00
55	TxSym10BurstCtrl	0x01	0x01
56	TxSym10Mod	0x01	0x01
57	TxSym32Mod	0x00	0x00
58	RxBitMod	0x18	0x18
59	RxEofSym	0x00	0x00
5A	RxSyncValH	0xB2	0xB2
5B	RxSyncValL	0x4D	0x4D
5C	RxSyncMod	0xF0	0xF0
5D	RxMod	0x19	0x19
5E	RxCorr	0x20	0x50
5F	RxSvette_Reg	0xF0	0xF0

4.5.2 FeliCa for ID2 sized antenna

Table 18. Register settings FeliCa ID2 sized antenna

	Reg	Reg descr	212 kbit/s	424 kbit/s
	28	DrvMode_Reg	0x8F	0x8F
	29	TxAmp_Reg	0x17	0x17
	2A	DrvCon_Reg	0x01	0x01
	2B	TxI_Reg	0x06	0x06
	2C	TXCrcCon	0x09	0x09
	2D	RxCrcCon	0x09	0x09
	2E	TxDataNum	0x08	0x08
	2F	TxModWidth	0x00	0x00
	30	TxSym10BurstLen	0x03	0x03
	31	TxWaitCtrl	0x80	0x80
	32	TxWaitLo	0x12	0x12
	33	TxFrameCon	0x01	0x01
	34	RXSOFD	0x00	0x00
	35	RxCtrl	0x05	0x06
	36	RxWait	0x10	0x40
	37	RxTreshold	0x3F	0x3F
	38	Rcv	0x12	0x12
	39	RxAna	0x02	0x02
TX_Protected	48	TxBitMod	0x80	0x80
	4A	TxDataCon	0x05	0x06
	4B	TxDataMod	0x01	0x01
	4C	TxSymFreq	0x05	0x06
	4D	TxSym0H	0xB2	0xB2
	4E	TxSym0L	0x4D	0x4D
	4F	TxSym1H	0x00	0x00
	50	TxSym1L	0x00	0x00
	51	TxSym2	0x00	0x00
	52	TxSym3	0x00	0x00
	53	TxSym10Len	0x0F	0x0F
	54	TxSym32Len	0x00	0x00
	55	TxSym10BurstCtrl	0x01	0x01
	56	TxSym10Mod	0x01	0x01
	57	TxSym32Mod	0x00	0x00
RX_Protected	58	RxBitMod	0x18	0x18
	59	RxEofSym	0x00	0x00
	5A	RxSyncValH	0xB2	0xB2
	5B	RxSyncValL	0x4D	0x4D
	5C	RxSyncMod	0xF0	0xF0
	5D	RxMod	0x19	0x19
	5E	RxCorr	0x20	0x50
	5F	RxSvette_Reg	0xF0	0xF0

4.5.3 FeliCa for ID3 sized antenna

Table 19. Register settings FeliCa ID3 sized antenna

Reg	Reg descr	212 kbit/s	424 kbit/s
28	DrvMode_Reg	0x8F	0x8F
29	TxAmp_Reg	0x17	0x17
2A	DrvCon_Reg	0x01	0x01
2B	TxI_Reg	0x0A	0x0A
2C	TXCrcCon	0x09	0x09
2D	RxCrcCon	0x09	0x09
2E	TxDataNum	0x08	0x08
2F	TxModWidth	0x00	0x00
30	TxSym10BurstLen	0x03	0x03
31	TxWaitCtrl	0x80	0x80
32	TxWaitLo	0x12	0x12
33	TxFrameCon	0x01	0x01
34	RXSOFD	0x00	0x00
35	RxCtrl	0x05	0x06
36	RxWait	0x10	0x40
37	RxTreshold	0x3C	0x3C
38	Rcv	0x12	0x12
39	RxAna	0x02	0x02
48	TxBitMod	0x80	0x80
4A	TxDataCon	0x05	0x06
4B	TxDataMod	0x01	0x01
4C	TxSymFreq	0x05	0x06
4D	TxSym0H	0xB2	0xB2
4E	TxSym0L	0x4D	0x4D
4F	TxSym1H	0x00	0x00
50	TxSym1L	0x00	0x00
51	TxSym2	0x00	0x00
52	TxSym3	0x00	0x00
53	TxSym10Len	0x0F	0x0F
54	TxSym32Len	0x00	0x00
55	TxSym10BurstCtrl	0x01	0x01
56	TxSym10Mod	0x01	0x01
57	TxSym32Mod	0x00	0x00
58	RxBitMod	0x18	0x18
59	RxEofSym	0x00	0x00
5A	RxSyncValH	0xB2	0xB2
5B	RxSyncValL	0x4D	0x4D
5C	RxSyncMod	0xF0	0xF0
5D	RxMod	0x19	0x19
5E	RxCorr	0x20	0x50
5F	RxSvette_Reg	0xF0	0xF0

4.6 ISO/IEC 15693 recommended register settings

The following section gives an overview of the recommended register settings for ISO/IEC 15693 communication, with different Antenna sizes (ID1, ID2, ID3).

4.6.1 ISO/IEC 15693 for ID1 sized antenna

Table 20. Register settings I-Code ID1 sized antenna

Reg	Reg descr	SLI ¼ SSC26	SLI ¼ SSC52	SLI 1/256 DSC
28	DrvMode_Reg	0x8F	0x8F	0x8E
29	TxAmp_Reg	0x4F	0x4F	0x4F
2A	DrvCon_Reg	0x01	0x01	0x01
2B	TxI_Reg	0x0A	0x0A	0x0A
2C	TXCrcCon	0x7B	0x7B	0x7B
2D	RxCrcCon	0x7B	0x7B	0x7B
2E	TxDataNum	0x08	0x08	0x08
2F	TxModWidth	0x00	0x00	0x00
30	TxSym10BurstLen	0x00	0x00	0x00
31	TxWaitCtrl	0x88	0x88	0x88
32	TxWaitLo	0xA9	0xA9	0xA9
33	TxFrameCon	0x0F	0x0F	0x0F
34	RXSOFD	0x00	0x00	0x00
35	RxCtrl	0x02	0x03	0x02
36	RxWait	0x10	0x10	0x10
37	RxTreshold	0x44	0x44	0x44
38	Rcv	0x12	0x12	0x12
39	RxAna	0x06	0x06	0x06
48	TxBitMod	0x00	0x00	0x00
4A	TxDataCon	0x83	0x83	0x93
4B	TxDataMod	0x04	0x04	0x04
4C	TxSymFreq	0x40	0x40	0x40
4D	TxSym0H	0x00	0x00	0x00
4E	TxSym0L	0x00	0x00	0x00
4F	TxSym1H	0x00	0x00	0x00
50	TxSym1L	0x00	0x00	0x00
51	TxSym2	0x84	0x84	0x81
52	TxSym3	0x02	0x02	0x02
53	TxSym10Len	0x00	0x00	0x00
54	TxSym32Len	0x37	0x37	0x37
55	TxSym10BurstCtrl	0x00	0x00	0x00
56	TxSym10Mod	0x00	0x00	0x00
57	TxSym32Mod	0x00	0x00	0x00
58	RxBitMod	0x00	0x00	0x00
59	RxEofSym	0x1D	0x1D	0x1D
5A	RxSyncValH	0x00	0x00	0x00
5B	RxSyncValL	0x01	0x01	0x01
5C	RxSyncMod	0x00	0x00	0x00
5D	RxMod	0x24	0x24	0x26
5E	RxCorr	0x60	0x40	0x60
5F	RxSvette_Reg	0xF0	0xF0	0xF0

4.6.2 ISO/IEC 15693 for ID2 sized antenna

Table 21. Register settings I-Code ID2 sized antenna

	Reg	Reg descr	SLI ¼ SSC26	SLI ¼ SSC52	SLI 1/256 DSC
	28	DrvMode_Reg	0x8F	0x8F	0x8E
	29	TxAmp_Reg	0x10	0x10	0x10
	2A	DrvCon_Reg	0x01	0x01	0x01
	2B	TxI_Reg	0x06	0x06	0x06
	2C	TXCrcCon	0x7B	0x7B	0x7B
	2D	RxCrcCon	0x7B	0x7B	0x7B
	2E	TxDataNum	0x08	0x08	0x08
	2F	TxModWidth	0x00	0x00	0x00
	30	TxSym10BurstLen	0x00	0x00	0x00
	31	TxWaitCtrl	0x88	0x88	0x88
	32	TxWaitLo	0xA9	0xA9	0xA9
	33	TxFrameCon	0x0F	0x0F	0x0F
	34	RXSOFD	0x00	0x00	0x00
	35	RxCtrl	0x02	0x03	0x02
	36	RxWait	0x10	0x10	0x10
	37	RxTreshold	0x44	0x44	0x44
	38	Rcv	0x12	0x12	0x12
	39	RxAna	0x06	0x06	0x06
TX_Protected	48	TxBitMod	0x00	0x00	0x00
	4A	TxDataCon	0x83	0x83	0x93
	4B	TxDataMod	0x04	0x04	0x04
	4C	TxSymFreq	0x40	0x40	0x40
	4D	TxSym0H	0x00	0x00	0x00
	4E	TxSym0L	0x00	0x00	0x00
	4F	TxSym1H	0x00	0x00	0x00
	50	TxSym1L	0x00	0x00	0x00
	51	TxSym2	0x84	0x84	0x81
	52	TxSym3	0x02	0x02	0x02
	53	TxSym10Len	0x00	0x00	0x00
	54	TxSym32Len	0x37	0x37	0x37
	55	TxSym10BurstCtrl	0x00	0x00	0x00
	56	TxSym10Mod	0x00	0x00	0x00
	57	TxSym32Mod	0x00	0x00	0x00
RX_Protected	58	RxBitMod	0x00	0x00	0x00
	59	RxEofSym	0x1D	0x1D	0x1D
	5A	RxSyncValH	0x00	0x00	0x00
	5B	RxSyncValL	0x01	0x01	0x01
	5C	RxSyncMod	0x00	0x00	0x00
	5D	RxMod	0x24	0x24	0x26
	5E	RxCorr	0x60	0x40	0x60
	5F	RxSvette_Reg	0xF0	0xF0	0xF0

4.6.3 ISO/IEC 15693 for ID3 sized antenna

Table 22. Register settings I-Code ID3 sized antenna

Reg	Reg descr	SLI ¼ SSC26	SLI ¼ SSC52	SLI 1/256 DSC
28	DrvMode_Reg	0x8F	0x8F	0x8E
29	TxAmp_Reg	0x17	0x17	0x17
2A	DrvCon_Reg	0x01	0x01	0x01
2B	TxI_Reg	0x0A	0x0A	0x0A
2C	TXCrcCon	0x7B	0x7B	0x7B
2D	RxCrcCon	0x7B	0x7B	0x7B
2E	TxDataNum	0x08	0x08	0x08
2F	TxModWidth	0x00	0x00	0x00
30	TxSym10BurstLen	0x00	0x00	0x00
31	TxWaitCtrl	0x88	0x88	0x88
32	TxWaitLo	0xA9	0xA9	0xA9
33	TxFrameCon	0x0F	0x0F	0x0F
34	RXSOFD	0x00	0x00	0x00
35	RxCtrl	0x02	0x03	0x02
36	RxWait	0x10	0x10	0x10
37	RxTreshold	0x44	0x44	0x44
38	Rcv	0x12	0x12	0x12
39	RxAna	0x06	0x06	0x06
48	TxBitMod	0x00	0x00	0x00
4A	TxDataCon	0x83	0x83	0x93
4B	TxDataMod	0x04	0x04	0x04
4C	TxSymFreq	0x40	0x40	0x40
4D	TxSym0H	0x00	0x00	0x00
4E	TxSym0L	0x00	0x00	0x00
4F	TxSym1H	0x00	0x00	0x00
50	TxSym1L	0x00	0x00	0x00
51	TxSym2	0x84	0x84	0x81
52	TxSym3	0x02	0x02	0x02
53	TxSym10Len	0x00	0x00	0x00
54	TxSym32Len	0x37	0x37	0x37
55	TxSym10BurstCtrl	0x00	0x00	0x00
56	TxSym10Mod	0x00	0x00	0x00
57	TxSym32Mod	0x00	0x00	0x00
58	RxBitMod	0x00	0x00	0x00
59	RxEofSym	0x1D	0x1D	0x1D
5A	RxSyncValH	0x00	0x00	0x00
5B	RxSyncValL	0x01	0x01	0x01
5C	RxSyncMod	0x00	0x00	0x00
5D	RxMod	0x24	0x24	0x26
5E	RxCorr	0x60	0x40	0x60
5F	RxSvette_Reg	0xF0	0xF0	0xF0

4.7 ISO18000-3 Mode3 recommended register settings

4.7.1 ISO18000-3 Mode3 ID1 sized antenna

Table 23. ISO18000-3 Mode3 ID1 sized antenna

Reg	Reg descr	EPC V2 2/424	EPC V2 4/424	EPC V2 2/848	EPC V2 4/848
28	DrvMode_Reg	0x8F	0x8F	0x8F	0x8F
29	TxAmp_Reg	0x4F	0x4F	0x4F	0x4F
2A	DrvCon_Reg	0x01	0x01	0x01	0x01
2B	TxI_Reg	0x0A	0x0A	0x0A	0x0A
2C	TXCrcCon	0x11	0x11	0x11	0x11
2D	RxCrcCon	0x91	0x91	0x91	0x91
2E	TxDataNum	0x09	0x09	0x09	0x09
2F	TxModWidth	0x00	0x00	0x00	0x00
30	TxSym10BurstLen	0x00	0x00	0x00	0x00
31	TxWaitCtrl	0x80	0x80	0x80	0x80
32	TxWaitLo	0x12	0x12	0x12	0x12
33	TxFrameCon	0x01	0x01	0x01	0x01
34	RXSOFD	0x00	0x00	0x00	0x00
35	RxCtrl	0x04	0x03	0x05	0x04
36	RxWait	0x00	0x00	0x00	0x00
37	RxTreshold	0x36	0x36	0x36	0x36
38	Rcv	0x12	0x12	0x12	0x12
39	RxAna	0x0A	0x0A	0x0A	0x0A
48	TxBitMod	0x80	0x80	0x80	0x80
4A	TxDataCon	0xC5	0xC5	0xC5	0xC5
4B	TxDataMod	0x00	0x00	0x00	0x00
4C	TxSymFreq	0x05	0x05	0x05	0x05
4D	TxSym0H	0x68	0x68	0x68	0x68
4E	TxSym0L	0x41	0x41	0x41	0x41
4F	TxSym1H	0x01	0x01	0x01	0x01
50	TxSym1L	0xA1	0xA1	0xA1	0xA1
51	TxSym2	0x00	0x00	0x00	0x00
52	TxSym3	0x00	0x00	0x00	0x00
53	TxSym10Len	0x8E	0x8E	0x8E	0x8E
54	TxSym32Len	0x00	0x00	0x00	0x00
55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
56	TxSym10Mod	0x00	0x00	0x00	0x00
57	TxSym32Mod	0x00	0x00	0x00	0x00
58	RxBitMod	0x08	0x08	0x08	0x08
59	RxEofSym	0x0B	0x0B	0x0B	0x0B
5A	RxSyncValH	0x00	0x00	0x00	0x00
5B	RxSyncValL	0x01	0x01	0x01	0x01
5C	RxSyncMod	0x04	0x04	0x04	0x04
5D	RxMod	0x0C	0x0C	0x0C	0x0C
5E	RxCorr	0x40	0x50	0x88	0x80
5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

4.7.2 ISO18000-3 Mode3 ID2 sized antenna

Table 24. ISO18000-3 Mode3 ID2 sized antenna

	Reg	Reg descr	EPC V2 2/424	EPC V2 4/424	EPC V2 2/848	EPC V2 4/848
	28	DrvMode_Reg	0x8F	0x8F	0x8F	0x8F
	29	TxAmp_Reg	0x10	0x10	0x10	0x10
	2A	DrvCon_Reg	0x01	0x01	0x01	0x01
	2B	TxI_Reg	0x06	0x06	0x06	0x06
	2C	TXCrcCon	0x11	0x11	0x11	0x11
	2D	RxCrcCon	0x91	0x91	0x91	0x91
	2E	TxDataNum	0x09	0x09	0x09	0x09
	2F	TxModWidth	0x00	0x00	0x00	0x00
	30	TxSym10BurstLen	0x00	0x00	0x00	0x00
	31	TxWaitCtrl	0x80	0x80	0x80	0x80
	32	TxWaitLo	0x12	0x12	0x12	0x12
	33	TxFrameCon	0x01	0x01	0x01	0x01
	34	RXSOFD	0x00	0x00	0x00	0x00
	35	RxCtrl	0x04	0x03	0x05	0x04
	36	RxWait	0x00	0x00	0x00	0x00
	37	RxTreshold	0x36	0x36	0x36	0x36
	38	Rcv	0x12	0x12	0x12	0x12
	39	RxAna	0x0A	0x0A	0x0A	0x0A
TX_Protected	48	TxBitMod	0x80	0x80	0x80	0x80
	4A	TxDataCon	0xC5	0xC5	0xC5	0xC5
	4B	TxDataMod	0x00	0x00	0x00	0x00
	4C	TxSymFreq	0x05	0x05	0x05	0x05
	4D	TxSym0H	0x68	0x68	0x68	0x68
	4E	TxSym0L	0x41	0x41	0x41	0x41
	4F	TxSym1H	0x01	0x01	0x01	0x01
	50	TxSym1L	0xA1	0xA1	0xA1	0xA1
	51	TxSym2	0x00	0x00	0x00	0x00
	52	TxSym3	0x00	0x00	0x00	0x00
	53	TxSym10Len	0x8E	0x8E	0x8E	0x8E
	54	TxSym32Len	0x00	0x00	0x00	0x00
	55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
	56	TxSym10Mod	0x00	0x00	0x00	0x00
	57	TxSym32Mod	0x00	0x00	0x00	0x00
RX_Protected	58	RxBitMod	0x08	0x08	0x08	0x08
	59	RxEofSym	0x0B	0x0B	0x0B	0x0B
	5A	RxSyncValH	0x00	0x00	0x00	0x00
	5B	RxSyncValL	0x01	0x01	0x01	0x01
	5C	RxSyncMod	0x04	0x04	0x04	0x04
	5D	RxMod	0x0C	0x0C	0x0C	0x0C
	5E	RxCorr	0x40	0x50	0x88	0x80
	5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

4.7.3 ISO18000-3 Mode3 ID3 sized antenna

Table 25. ISO18000-3 Mode3 ID3 sized antenna

Reg	Reg descr	EPC V2 2/424	EPC V2 4/424	EPC V2 2/848	EPC V2 4/848
28	DrvMode_Reg	0x8F	0x8F	0x8F	0x8F
29	TxAmp_Reg	0x17	0x17	0x17	0x17
2A	DrvCon_Reg	0x01	0x01	0x01	0x01
2B	TxI_Reg	0x0A	0x0A	0x0A	0x0A
2C	TXCrcCon	0x11	0x11	0x11	0x11
2D	RxCrcCon	0x91	0x91	0x91	0x91
2E	TxDataNum	0x09	0x09	0x09	0x09
2F	TxModWidth	0x00	0x00	0x00	0x00
30	TxSym10BurstLen	0x00	0x00	0x00	0x00
31	TxWaitCtrl	0x80	0x80	0x80	0x80
32	TxWaitLo	0x12	0x12	0x12	0x12
33	TxFrameCon	0x01	0x01	0x01	0x01
34	RXSOFD	0x00	0x00	0x00	0x00
35	RxCtrl	0x04	0x03	0x05	0x04
36	RxWait	0x00	0x00	0x00	0x00
37	RxTreshold	0x36	0x36	0x36	0x36
38	Rcv	0x12	0x12	0x12	0x12
39	RxAna	0x0A	0x0A	0x0A	0x0A
48	TxBitMod	0x80	0x80	0x80	0x80
4A	TxDataCon	0xC5	0xC5	0xC5	0xC5
4B	TxDataMod	0x00	0x00	0x00	0x00
4C	TxSymFreq	0x05	0x05	0x05	0x05
4D	TxSym0H	0x68	0x68	0x68	0x68
4E	TxSym0L	0x41	0x41	0x41	0x41
4F	TxSym1H	0x01	0x01	0x01	0x01
50	TxSym1L	0xA1	0xA1	0xA1	0xA1
51	TxSym2	0x00	0x00	0x00	0x00
52	TxSym3	0x00	0x00	0x00	0x00
53	TxSym10Len	0x8E	0x8E	0x8E	0x8E
54	TxSym32Len	0x00	0x00	0x00	0x00
55	TxSym10BurstCtrl	0x00	0x00	0x00	0x00
56	TxSym10Mod	0x00	0x00	0x00	0x00
57	TxSym32Mod	0x00	0x00	0x00	0x00
58	RxBitMod	0x08	0x08	0x08	0x08
59	RxEofSym	0x0B	0x0B	0x0b	0x0B
5A	RxSyncValH	0x00	0x00	0x00	0x00
5B	RxSyncValL	0x01	0x01	0x01	0x01
5C	RxSyncMod	0x04	0x04	0x04	0x04
5D	RxMod	0x0C	0x0C	0x0C	0x0C
5E	RxCorr	0x40	0x50	0x88	0x80
5F	RxSvette_Reg	0xF0	0xF0	0xF0	0xF0

5. References

[1] Product Data Sheet; CLRC663 Contactless reader IC (Doc. Nr.:1711xx)

[2] Application note; AN11019 CLRC663 Antenna Design Guide (Doc. Nr.:2058xx)

[3] Application note; AN11116 (“Using the RS232 serial evaluation boards on a USB port”), (Doc. Nr.:2151xx)

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7. List of figures

8. List of tables

9. Contents

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